

CD4099BC 8-Bit Addressable Latch

General Description

The CD4099BC is an 8-bit addressable latch with three address inputs (A0–A2), an active low enable input (\bar{E}), active high clear input (CL), a data input (D), and eight outputs (Q0–Q7).

Data is entered into a particular bit in the latch when that bit is addressed by the address inputs and the enable (\bar{E}) is LOW. Data entry is inhibited when enable (\bar{E}) is HIGH.

When clear (CL) and enable (\bar{E}) are HIGH, all outputs are LOW. When clear (CL) is HIGH and enable (\bar{E}) is LOW, the channel demultiplexing occurs. The bit that is addressed has an active output which follows the data input while all unaddressed bits are held LOW. When operating in the addressable latch mode ($\bar{E} = \text{CL} = \text{LOW}$), changing more than one bit of the address could impose a transient wrong address. Therefore, this should only be done while in the memory mode ($\bar{E} = \text{HIGH}$, $\text{CL} = \text{LOW}$).

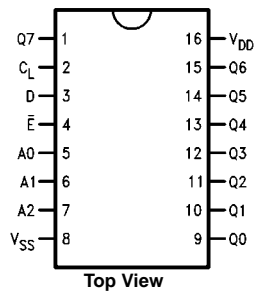
Features

- Wide supply voltage range: 3.0V to 15V
- High noise immunity: $0.45 V_{DD}$ (typ.)
- Low power TTL: fan out of 2 driving 74L compatibility: or 1 driving 74LS
- Serial to parallel capability
- Storage register capability
- Random (addressable) data entry
- Active high demultiplexing capability
- Common active high clear

Ordering Code:

Order Number	Package Number	Package Description
CD4099BCN	N16E	16-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-001, 0.300" Wide

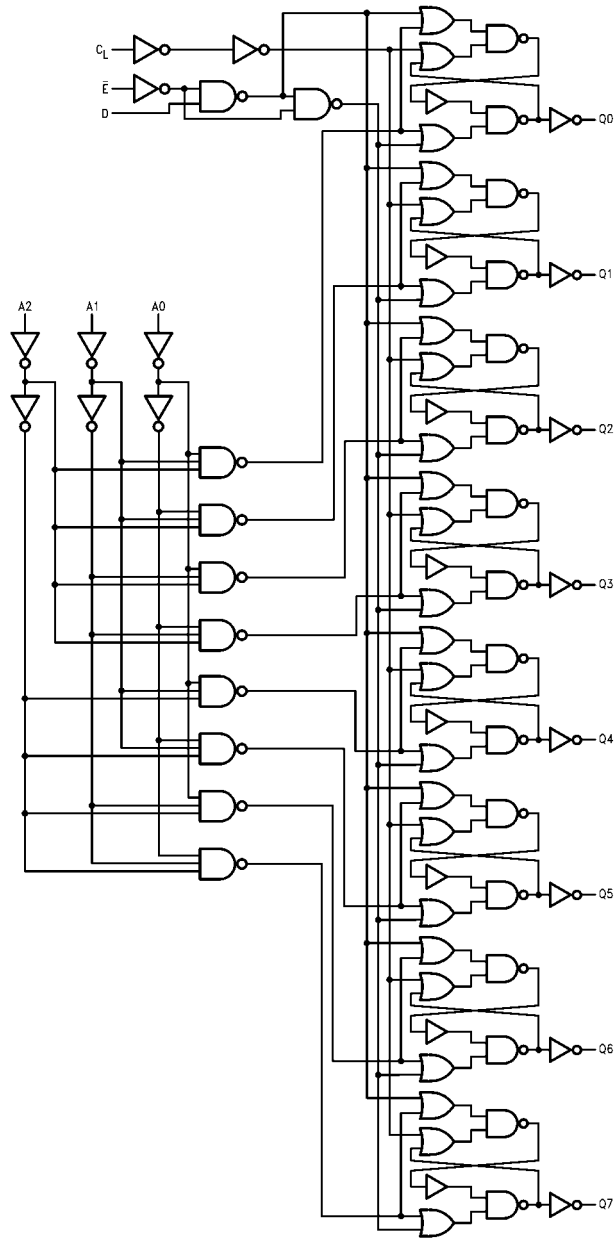
Connection Diagram



Truth Table

Mode Selection				
\bar{E}	CL	Addressed Latch	Unaddressed Latch	Mode
L	L	Follows Data	Holds Previous Data	Addressable Latch
H	L	Holds Previous Data	Holds Previous Data	Memory
L	H	Follows Data	Reset to "0"	Demultiplexer
H	H	Reset to "0"	Reset to "0"	Clear

Logic Diagram



Absolute Maximum Ratings <small>(Note 1)</small>		Recommended Operating Conditions <small>(Note 2)</small>	
DC Supply Voltage (V_{DD})	-0.5 to +18 V_{DC}	DC Supply Voltage (V_{DD})	3.0 to 15 V_{DC}
Input Voltage (V_{IN})	-0.5 to $V_{DD} + 0.5 V_{DC}$	Input Voltage (V_{IN})	0 to $V_{DD} V_{DC}$
Storage Temperature Range (T_S)	-65°C to +150°C	Operating Temperature Range (T_A)	-55°C to +125°C
Power Dissipation (P_D)		Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed; they are not meant to imply that the devices should be operated at these limits. The tables of "Recommended Operating Conditions" and "Electrical Characteristics" provide conditions for actual device operation.	
Dual-In-Line	700 mW	Note 2: $V_{SS} = 0V$ unless otherwise specified.	
Small Outline	500 mW		
Lead Temperature (T_L) (Soldering, 10 seconds)	260°C		

DC Electrical Characteristics (Note 2)

Symbol	Parameter	Conditions	-55°C		+25°C			+125°C		Units
			Min	Max	Min	Typ	Max	Min	Max	
I_{DD}	Quiescent Device Current	$V_{DD} = 5V, V_{IN} = V_{DD} \text{ or } V_{SS}$		5.0		0.02	5.0		150	μA
		$V_{DD} = 10V, V_{IN} = V_{DD} \text{ or } V_{SS}$		10		0.02	10		300	
		$V_{DD} = 15V, V_{IN} = V_{DD} \text{ or } V_{SS}$		20		0.02	20		600	
V_{OL}	LOW Level Output Voltage	$ I_{OL} \leq 1 \mu A$								V
		$V_{DD} = 5V$		0.05		0	0.05		0.05	
		$V_{DD} = 10V$		0.05		0	0.05		0.05	
V_{OH}	HIGH Level Output Voltage	$ I_{OL} \leq 1 \mu A$								V
		$V_{DD} = 5V$	4.95		4.95	5		4.95		
		$V_{DD} = 10V$	9.95		9.95	10		9.95		
V_{IL}	LOW Level Input Voltage	$V_{DD} = 5V, V_O = 0.5V \text{ or } 4.5V$		1.5		2.25	1.5		1.5	V
		$V_{DD} = 10V, V_O = 1.0V \text{ or } 9.0V$		3.0		4.5	3.0		3.0	
		$V_{DD} = 15V, V_O = 1.5V \text{ or } 13.5V$		4.0		6.75	4.0		4.0	
V_{IH}	HIGH Level Input Voltage	$V_{DD} = 5V, V_O = 0.5V \text{ or } 4.5V$	3.5		3.5	2.75		3.5		V
		$V_{DD} = 10V, V_O = 1.0V \text{ or } 9.0V$	7.0		7.0	5.5		7.0		
		$V_{DD} = 15V, V_O = 1.5V \text{ or } 13.5V$	11.0		11.0	8.25		11.0		
I_{OL}	LOW Level Output Current (Note 3)	$V_{DD} = 5V, V_O = 0.4V$	0.64		0.51	0.88		0.36		mA
		$V_{DD} = 10V, V_O = 0.5V$	1.6		1.3	2.25		0.9		
		$V_{DD} = 15V, V_O = 1.5V$	4.2		3.4	8.8		2.4		
I_{OH}	HIGH Level Output Current (Note 3)	$V_{DD} = 5V, V_O = 4.6V$	-0.64		-0.51	-0.88		-0.36		mA
		$V_{DD} = 10V, V_O = 9.5V$	-1.6		-1.3	-2.25		-0.9		
		$V_{DD} = 15V, V_O = 13.5V$	-4.2		-3.4	-8.8		-2.4		
I_{IN}	Input Current	$V_{DD} = 15V, V_{IN} = 0V$		-0.1		-10^{-5}	-0.1		-1.0	μA
		$V_{DD} = 15V, V_{IN} = 15V$		0.1		10^{-5}	0.1		1.0	

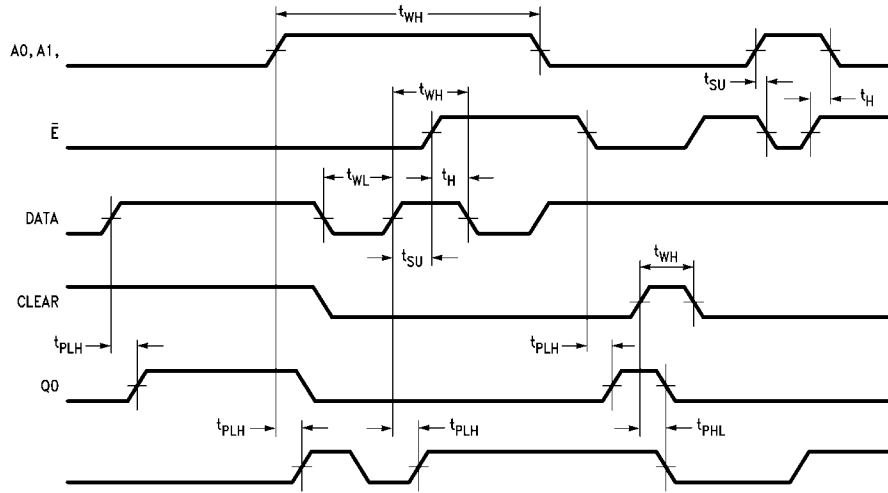
Note 3: I_{OH} and I_{OL} are tested one output at a time.

AC Electrical Characteristics (Note 4)						
T _A = 25°C, C _L = 50 pF, R _L = 200k, Input t _r = t _f = 20 ns, unless otherwise noted						
Symbol	Parameter	Conditions	Min	Typ	Max	Units
t _{PHL} , t _{PLH}	Propagation Delay Data to Output	V _{DD} = 5V V _{DD} = 10V V _{DD} = 15V		200 75 50	400 150 100	ns
t _{PLH} , t _{PHL}	Propagation Delay Enable to Output	V _{DD} = 5V V _{DD} = 10V V _{DD} = 15V		200 80 60	400 160 120	ns
t _{PHL}	Propagation Delay Clear to Output	V _{DD} = 5V V _{DD} = 10V V _{DD} = 15V		175 80 65	350 160 130	ns
t _{TLH} , t _{THL}	Propagation Delay Address to Output	V _{DD} = 5V V _{DD} = 10V V _{DD} = 15V		225 100 75	450 200 150	ns
t _{THL} , t _{TLH}	Transition Time (Any Output)	V _{DD} = 5V V _{DD} = 10V V _{DD} = 15V		100 50 40	200 100 80	ns
T _{WH} , T _{WL}	Minimum Data Pulse Width	V _{DD} = 5V V _{DD} = 10V V _{DD} = 15V		100 50 40	200 100 80	ns
t _{WH} , t _{WL}	Minimum Address Pulse Width	V _{DD} = 5V V _{DD} = 10V V _{DD} = 15V		200 100 65	400 200 125	ns
t _{WH}	Minimum Clear Pulse Width	V _{DD} = 5V V _{DD} = 10V V _{DD} = 15V		75 40 25	150 75 50	ns
t _{SU}	Minimum Set-Up Time Data to E	V _{DD} = 5V V _{DD} = 10V V _{DD} = 15V		40 20 15	80 40 30	ns
t _H	Minimum Hold Time Data to E	V _{DD} = 5V V _{DD} = 10V V _{DD} = 15V		60 30 25	120 60 50	ns
t _{SU}	Minimum Set-Up Time Address to E	V _{DD} = 5V V _{DD} = 10V V _{DD} = 15V		-15 0 0	50 30 20	ns
t _H	Minimum Hold Time Address to E	V _{DD} = 5V V _{DD} = 10V V _{DD} = 15V		-50 -20 -15	15 10 5	ns
C _{PD}	Power Dissipation Capacitance	Per Package (Note 5)		100		pF
C _{IN}	Input Capacitance	Any Input		5.0	7.5	pF

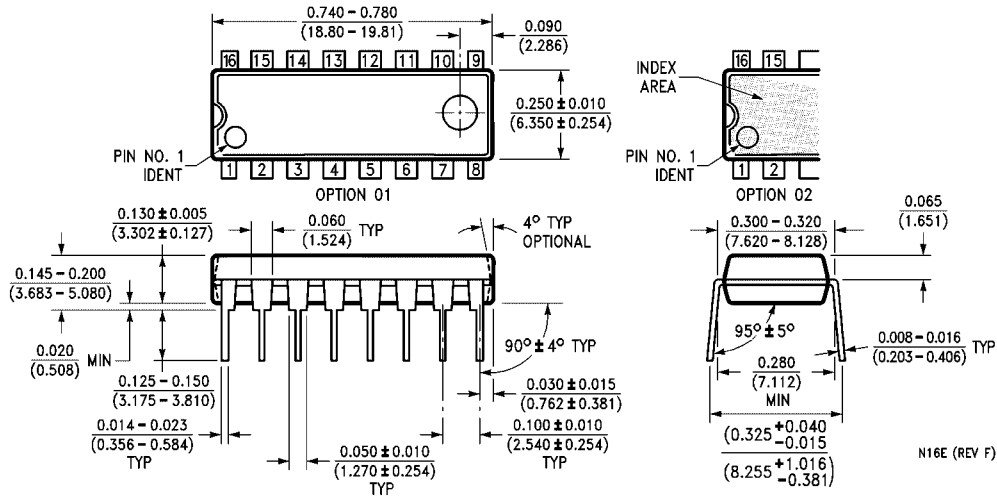
Note 4: AC Parameters are guaranteed by DC correlated testing.

Note 5: Dynamic power dissipation (P_D) is given by: P_D = (C_{PD} + C_L) V_{CC}²f + P_{CI}; where C_L = load capacitance; f = frequency of operation; for further details, see application note AN-90, "54C/74C Family Characteristics".

Switching Time Waveforms



Physical Dimensions inches (millimeters) unless otherwise noted



16-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-001, 0.300" Wide Package Number N16E

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